

Abstract

A designer configurable processor for a single or multi-processing system is described. The processor includes a plurality of designer configurable computational units, such as Very Long Instruction Word (VLIW) processor task engine, that operate in parallel. A memory device communicates with the plurality of computational units through a data communication module. The memory device stores at least one of data and instruction code. A software development tool, which can include a compiler, an assembler, an instruction set simulator, or a debugging environment, configures the plurality of computational units. The software development tool configures various aspects of the processor architecture and various operating parameters of the processor and can generate a synthesizable RTL description of the processor and a single or multi-processing system.

2000626_1